4511 East Paris S.E. ● Grand Rapids, MI 49512 ● Tel. (616) 554-9820, Fax (616) 554-9821

Statement of Work

PWB-IPC-6012

For

Printed Wiring Boards

Table of Contents

4511 East Paris S.E. ● Grand Rapids, MI 49512 ● Tel. (616) 554-9820, Fax (616) 554-9821

1.0 PURPOSE

The purpose of this Statement of Work is to provide our Supplier with the minimum requirements and instructions to comply with the Purchase Order on which it is referenced.

2.0 SCOPE

This Statement of Work is applicable to all Purchase Orders for the Procurement of Printed Wiring Boards (PWB). This Statement of Work applies to all Purchase Orders purchased after the release date of the current revision. The Printed Wiring Boards shall meet the requirements of IPC-6012 Class II when no other document states otherwise. Documentation precedence is set by the sort order in the ABT BOM. Any questions related to precedence need to be directed to ABT Engineering at: "Grand Rapids - Tooling GR_Tooling@borisch.com".

3.0 REFERENCES

IPC-6012 QUALIFICATION AND PERFORMANCE SPECIFICATION FOR RIGID PRINTED BOARDS

IPC-A-600 ACCEPTABILITY OF PRINTED BOARDS

IPC-9252 GUIDELINES AND REQUIREMENTS FOR ELECTRICAL TESTING OF UNPOPULATED PRINTED BOARDS

4.0 PWB Array DFM

4.1 **General** - The following specifications and guidelines *are required to* be used in the DFM process for all PWB procured by Amphenol Borisch Technologies (ABT).
All PWB with any of the following conditions shall be delivered as an array:

- 4.1.1 Component to board edge set back is less than 0.250"on two parallel sides. Rails are required *on the two longest* sides at minimum.
- 4.1.2 The PWB design contains no two parallel sides.
- 4.1.3 The PWB construction requires semi-rigid and/or flexible material.
- 4.1.4 It is economically applicable.
- 4.1.5 If an economical array solution cannot be achieved per this document, the Supplier shall develop a solution with ABT.
- *4.1.6 Rigid flex arrays cannot be larger than 2 up. 1up in a full frame is preferred.*
- *4.1.7 Flex arrays cannot be larger than 2 up. 1up in a full frame is preferred*
  - *4.1.7.1 Flex array frame is preferred with a rigid backer when single sided*

4.2 **PWB Array Configuration**

4.2.1 **Printed Wiring Board Outline** – Where possible, the shape of an PWB array shall be square or rectangular in nature.

4.2.2 **Minimum and Maximum Array Sizes** – The minimum array size shall be 4.00" long x 4.00" wide for all board thicknesses, the maximum array size shall be 10.00" long x 8.00" wide for board thickness that are 0.062" or less and 16.00" long x 12.00" wide for board thicknesses greater than 0.062".

4.2.3 **Minimum Array Margins** – The minimum Array margin from the outer Array edge to the nearest routed slot is 0.300".

4.2.4 **Route Guidelines –** All PWB shall exhibit tabbed 0.093" route between PWB and Array Frame. No mouse bites, No V-Score

4.2.5 Copper thieving – Circular, Dot, etc thieving is NOT allowed, on the top or bottom layer. Use Diamond, Square, or hatch Thieving.

4.3 **Irregular Shapes -** All PWB with irregular shapes shall have all open voids filled with material, (reference Figure 1, para 4.5).

4.4 **Tooling Hole Locations –** Four non-plated tooling holes, 0.125" diameter, are required to be located at the center of all four corners of Array. (ref Figure 1, para 4.5).

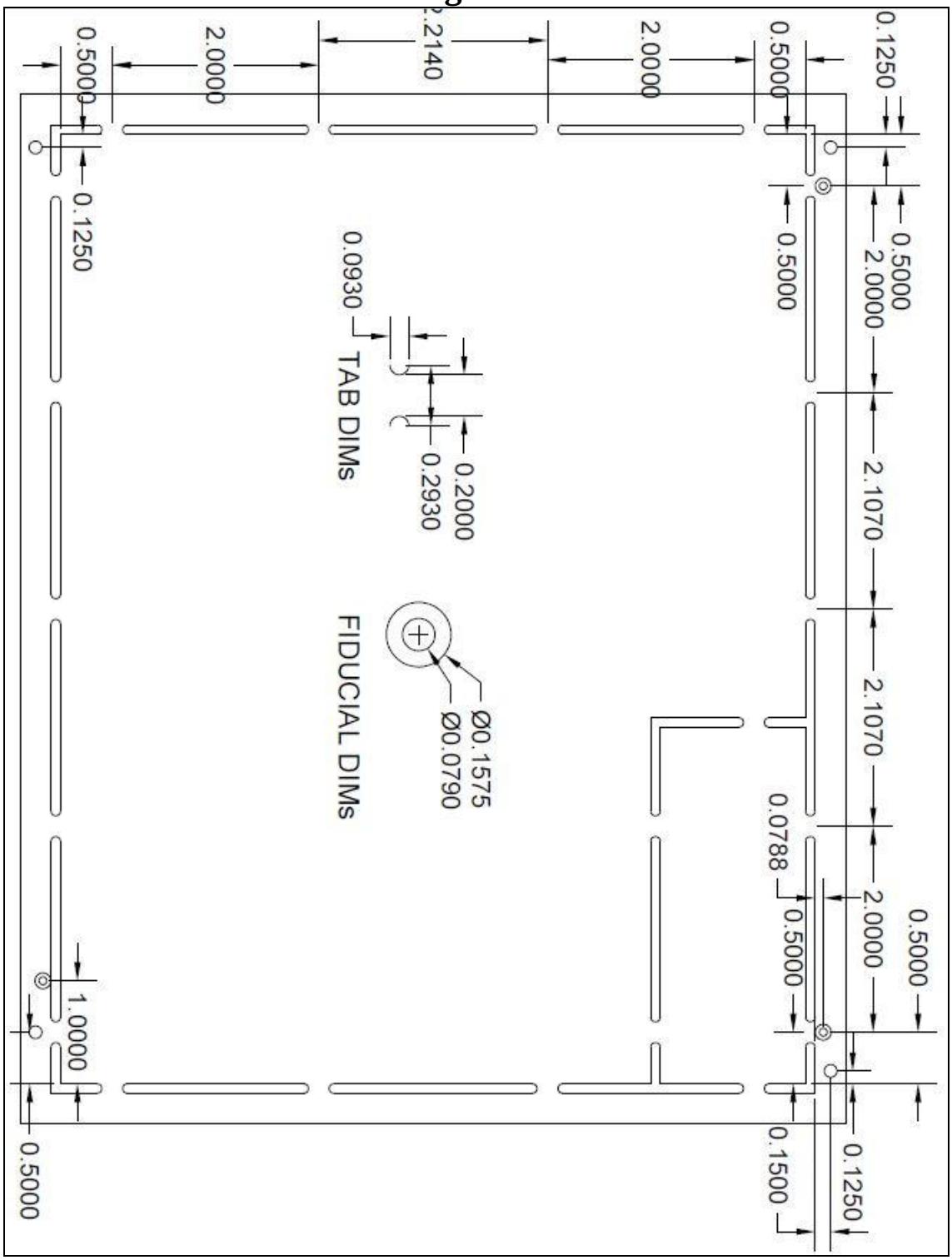
4.4.1 One corner must have the tooling hole swapped with the Fiducial to make the alignment non-symmetrical

4.5 **Global Array Fiducial Marks –** All Arrays must include three global Array fiducials, 0.079" diameter pad with a 0.1575" diameter clearance to be located per Figure 1 below.

4.5.1 The fiducials are NOT to be centered on the rail. They need to be justified to the inside.

4511 East Paris S.E. ● Grand Rapids, MI 49512 ● Tel. (616) 554-9820, Fax (616) 554-9821

Figure 1



4.6 **Customer Approval Process –** Upon completion of PWB Array layout, Gerber files must be submitted to ABT for approval, by emailing them to "Grand Rapids - Tooling GR_Tooling@borisch.com". All PWB Array layout Gerber files shall be formatted as follows: .art, .gbx, .ger, .rs-274-x, .tar or similar formats. Upon submission, the proposed "unapproved" panel must be reviewed by ABT SMT manufacturing. This process shall be completed prior to the PWB Supplier proceeding with developing tooling and/or production.

4.6.1 **Panel Approval process:**

4.6.1.1 PO is issued against panel PN listed on ABT BOM

4.6.1.1.1 ABT BOM Panel PN Example: BMCXXXXXPRA

4.6.1.2 Board supplier reviews all documentation sent with the PO and develops an array (Panel) proposal.

4.6.1.2.1 Files are to be named: "BMCXXXXXPRA_Unapproved_01"

4.6.1.3 Board supplier sends proposed Panel to customer (ABT) for approval.

4.6.1.3.1 If adjustments are requested by the customer (ABT), the unapproved revision will increment when the file is resubmitted for approval.

4.6.1.3.1.1 Example: "BMCXXXXXPRA_Unapproved_02"

4.6.1.3.2 If the proposal is approved the customer (ABT) will send an email with approval and the file attached with the Unapproved portion removed.

4.6.1.3.2.1 Example File Name: "BMCXXXXXPRA"

4.6.1.3.2.2 Example Email Body: "This panel is approved."

5.0 REQUIREMENTS

5.1 **General** - All PWB required to comply with this Statement of Work must be Manufactured, Processed, Inspected, Tested and Marked (Identified) in accordance with IPC-6012, CLASS II. All boards must be marked with the date code.

NOTE*:* Should another Specification or classification be required by the Procurement Documentation/Drawing, the Procurement Documentation/Drawing will take precedence.

5.2 **Acceptance** - As applicable, the PWB shall meet the requirements of IPC-A-600.

5.3 **Electrical Testing** - Continuity and Isolation shall be performed in accordance with IPC-9252.

5.3.1 **Continuity –** Testing shall be performed using the Gerber Net List Test method in accordance with IPC-9252.

Amphenol BORISCH TECHNOLOGIES

4511 East Paris S.E. ● Grand Rapids, MI 49512 ● Tel. (616) 554-9820, Fax (616) 554-9821

5.4 Cleanliness Requirement –

5.4.1 Boards with HASL finish will require the following information be communicated to ABT:

5.4.1.1 The flux TDS, Flux application method, HASL machine/process

5.4.1.2 Wash process specifications, including (but not limited too) Pre-wash and final wash water sources

5.4.2 Full board extraction Ion Chromatography – validated proof using test method IPC TM 650 2.3.28

5.4.2.1 Using an appropriate amount of solution: a target ratio of 1:1

5.4.2.1.1 Example: 4”x4” = 20 ml of solution

5.4.2.2 Limits are given in the chart below.

		Fluoride	Acetate	Formate	Methane Sulfonic Acid	Chloride	Nitrate	Bromide	Nitrite	Phosphate	Sulfate	Weak Organic Acid	Weak Organic Acid	Lithium	Sodium	Potassium	Ammonium	Calcium	Magnesium	C3 - Class 2 & 3	C3 - Class 1
		F^-	$C_2H_3O_2$	HCO_2^-	MSA	Cl^-	NO_3^-	Br^-	NO_2^-	PO_4^{3-}	SO_4^{2-}	SMT hand & selective	Wave direct contact	Li^+	Na^+	K^+	NH_4^+	Ca^{2+}	Mg^{2+}	time / µA	time / µA
Component	BGA Reballed BGA Tinned IC Flip Chip Trayed Component	1	3	1	1	1	2	6	2	2	1	25	n/a	1	2	2	2.5	n/a	n/a	>120s / 250µA	>60s / 500µA
PCBA (no clean)	NC Via Top Solder Area NC SMT NC Wave Reworked	1	3	3	1	3	3	6	3	3	3	25	150	3	3	3	3	n/a	n/a	>120s / 250µA	>60s / 500µA
PCBA (clean)	NC / WSF Via Top Selective NC / WSF SMT NC / WSF Wave Rework / Misprint	1	3	3	1	6	3	6	3	3	3	25	25	3	3	3	3	n/a	n/a	>120s / 250µA	>60s / 500µA
Support Hardware	Heat Sink Housing / ESD Foam Thermal Material Thermal Pad Battery Housing	1	3	3	1	2	3	6	3	3	3	n/a	n/a	1	1	3	2	n/a	n/a	>120s / 250µA	>60s / 500µA

5.4.2.3 No substitution of Rose testing (IPC TM 650 2.3.25) without formal discussion and approval given by ABT SMT manufacturing group.

5.5 **Micro Sections** - Each lot shall have micro section evaluations performed for hole integrity and verification of plating thickness. Micro sections must be shipped with each lot or with the first lot of each date code shipped. Micro sections will be retained by ABT for a minimum of 10 years unless otherwise requested in writing by the seller.

5.5.1 Micro sections used for evaluation by seller must be obtained from the actual lot produced and cannot be taken from other production lots.

5.5.2 Prior to micro sectioning the seller is to perform the required thermal stress testing in accordance with IPC-6012 samples will then be subjected to the test per paragraph 3.6.1of IPC-6012.

5.5.3 Coupons, Micro Sections and PWBs must be serialized (by array) for traceability.

5.5.4 Supplier is required to perform 100% inspection of the circuitry for all layers using AOI methods.

5.6 **Failures -** Each X-out board shall be marked in a manner that makes the X-out obvious. Markings must be permanent and if the board is two sided must be applied to both sides.

5.6.1 Each PWB that is intended to be an X-out shall be conspicuously and permanently identified.

5.6.2 The use of permanent markers (such as a Sharpie ®) is not considered permanent identification.

5.6.3 X-out thresholds must meet the following.

5.6.3.1 Single up panel: NO X-outs allowed.
5.6.3.2 Two up panel: 50% of the panel, 10% of lot.
5.6.3.3 Three up panel: 33% of the panel, 10% of the lot.
5.6.3.4 Four up panel: 25% of the panel, 15% of the lot.
5.6.3.5 Five or more panel: 20% of the panel, 20% of the lot.

5.6.3.6 All panels that do not meet this criterion can ONLY be shipped and invoiced at material cost.

5.6.3.7 By agreeing to the panel layout, the PWB supplier agrees to produce the PWB to the standards in the approved layout and will absorb any tooling and scrap costs associated with retooling a panel to meet quality and X-out requirements.

5.6.4 Arrays that include X-outs shall be segregated from non X-outs panels when being packaged for shipment. FIFO by DOM and lot is to be followed when shipping non X-out and X-out panels.

5.6.5 Each sealed package within the shipping container shall indicate the quantity of X-out boards and the quantity good usable boards.

5.6.6 Accompanying shipment paperwork shall indicate the quantity of X-out boards and the quantity good usable boards in each shipment.

5.6.7 PWBs being sent out to a refinish supplier after their original manufacturing shall continue to keep PWBs segregated and documented above. This process is required to be meet all specifications and documentation in section 5.4.

5.7 **Data Retention** - Documentation and data must be maintained by the Supplier for a period of 10 years, or as required by internal procedures, whichever is greater. In the case where a supplier goes out of business the documentation must be transferred by a ITAR approved method to ABT.

5.8 **Packaging** - The PWB shall be packaged in such a way that will prevent damage during shipping and storage. The PWB must be packaged in VACUUMED, HEAT SEALED MOISTURE BARRIER BAG.

5.8.1 All packaging shall contain a humidity indicator card (HIC) & desiccant.
5.8.1.1 The

5.8.2 Desiccants shall be located on the edges of the PWB, NOT on the PWB surface.

5.9 **Repair Authorization** – All repairs not covered (authorized) by specifications and documentation in section 5.4 require written approval of the ABT Quality Manager.

5.9.1 All reworked panels are required to be packaged separately from non-reworked panels.

5.9.2 All reworked panel shipments are required to be clearly marked or identified on paperwork.

6.0 CERTIFICATION

6.1 **Requirements** - In addition to the certification requirements listed on the purchase order the certification must reflect the date code and indicate the quantity in the shipment that passed the required Net List testing. Certification must reflect the number of boards tested and the quantity that passed and failed. Certification must also include the results of the evaluation of the micro section inspections.

4511 East Paris S.E. ● Grand Rapids, MI 49512 ● Tel. (616) 554-9820, Fax (616) 554-9821

PLEASE CONTACT THE ABT QUALITY MANAGER AND ABT SMT ENGINEERING WITH ADDITIONAL QUESTIONS.

yellow is used to indicate changes.

REV.	DESCRIPTION
B	Update SOW with superseded spec, added cover page, approval page and table of contents.
C	Added V-Score and Laser marking silkscreen requirements and AOI requirements
D	Added 4.8 Gerber archiving process & updated 4.5 to indicate must for 3 Array fids. Added 5.1.3.1 and 5.1.3.2 for X-outs
E	Added 5.1.3.1.1 thru 5.1.3.1.4, 5.1.3.2.1, 5.1.3.2.2 and 5.1.3.3
F	Revised V-Score to Route and removed '(example: 2x3 array, v-score)' from the end of paragraph 4.8, changed rail size, updated figure 1, added provision for development of economical array, removed page numbers form Table of Contents, removed 4.6 and 4.8, add flex PWB to array requirement, remove rigid notation
G	Sections 5.4, 5.5, 5.6, 5.7, 5.8 all bump by one to make a new 5.4 Section 5.4 Cleanliness Requirements, Added Scope update: Adds GR_tooling email group and "otherwise" statement 4.1.6, 4.1.7 updated to min/max 2 up and full frame 4.2.4, updated to no mouse bites and no V-score 4.2.5, updated/created to indicate thieving restrictions 4.4, updated added 4.4.1 for asymmetrical layout 4.5, updated added 4.5.1 fid center location on scrap rail Figure 1: updated panel drawing example with tab and fid detail 4.6, updated to include GR tooling group email. Added panel approval process 5.6.3 updated X-out acceptable percentages by panel UP size and lot 5.6.4 Added FIFO call out 5.6.7 added reference to 5.4 5.7 Added out of business case scenario 5.9 updated rework requirements and shipping segregation. Final note added ABT SMT engineering to statement

4511 East Paris S.E. ● Grand Rapids, MI 49512 ● Tel. (616) 554-9820, Fax (616) 554-9821

PREPARED BY	CHECKED BY	QA APPROVED	DATE
H.MACNAUGHTON Q.C. Engineer	S. MILLER Dir. of Engineering	J. PELLERITO Quality Manager	March 4, 2008
P. HUNTOON Spc Ops Engineer	S. MILLER Dir. of Engineering	J. PELLERITO Quality Manager	August 31, 2011
P. HUNTOON Spc Ops Engineer	S. MILLER Dir. of Engineering	J. PELLERITO Quality Manager	October 13, 2012
F. DORE Senior Mfg Engineer	S. MILLER Dir. of Engineering	B. GEROU Quality Engineer	February 17, 2015
S. Javor Senior Mfg. Engineer	S. MILLER Dir. of Engineering	J. PELLERITO Quality Manager	November 9, 2018
S. Black Sr. Mfg. Engineer			